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Donghong Cui

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10/26/2005

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IP DOCKET

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EXAMINER

NGUYEN, LINH V

ART UNIT

PAPER NUMBER

2819

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/759,173

Applicant(s)

CUI ET AL.

Examiner

Linh V. Nguyen

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 29 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-79 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-15 is/are allowed.
- 6) ☒ Claim(s) 1-19, 22, 24-32, 34 and 36-44 is/are rejected.
- 7) ☒ Claim(s) 20, 21, 23, 33 and 35 is/are objected to.
- 8) ☒ Claim(s) 45-79 are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 1/20/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

1. This office action is in response to applicant's communication filed on 9/29/05. Claims 1-44 and 74-79 have elected for examination. Claims 45 – 69 have withdraw with traverse.

### ***Specification***

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Examiner's Comment***

3. There is an error from previous restriction requirement: claims 74 – 79 belong to group II (instead of group I) for drawing to Fig. 2 of claimed invention. Applicant has elected Group I to for examination; therefore in this office action, claims 74 – 79 are withdraw also.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

Art Unit: 2819

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 16 – 19, 26, 29, 30, 31, 32 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Wiese et al. U.S. Patent No. 5,936,468.

Regarding claim 16, Fig. 1 of Wiese et al. discloses an electrical circuit, comprising: an amplifier, comprising: an input circuit (1, 2) in communication with an input of the amplifier (5, 6); a start-up circuit (3, 4) in communication with the input circuit, wherein the start-up circuit is configured to generate a start-up signal (11, 12) to enable subsequent operation of the amplifier; and an output circuit (18, 19, 20, 21, 23, 24, 30, 31) in communication with an output of the amplifier (32) and in communication with the input circuit (1, 2) and the start-up circuit (3, 4).

Regarding claim 17, wherein the amplifier comprises a differential amplifier (1, 2), wherein the input of the amplifier comprises a differential input (5, 6), and wherein the output of the amplifier comprises a differential output (32).

Regarding claim 18, wherein the input circuit comprises: a first input transistor (1); and a second input transistor (2), wherein base electrodes of the first and second input transistors are in communication with the input (5, 6), and wherein emitter electrodes of the first and second input transistors are in communication with each other and a first current source (13).

Regarding claim 19, wherein the start-up circuit (3, 4) comprises: a first start-up transistor (3), and a second start-up transistor (4), wherein base electrodes of the first

Art Unit: 2819

and second start-up transistors (3, 4) are in communication with a bias input (input at the base of 3, 4), wherein emitter electrodes of the first and second start-up transistors are in communication with each other and with a first current source (14), and wherein collector electrodes of the first and second start-up transistor are in communication with collector electrodes of first and second input transistors (11, 12), respectively.

Regarding claim 26, wherein the amplifier comprises a fully differential operational amplifier (Fig. 1).

Regarding claim 29, the claim incorporated similar subject matter as of claim 16, and rejected along the same rationale.

Regarding claim 30, wherein the amplifier means (Fig. 1) comprises a differential amplifier means (Fig. 1), wherein the input means (5, 6) of the amplifier means comprises a differential input means (5, 6), and wherein the output means of the amplifier means comprises a differential output means (32).

Regarding claim 31, wherein the input circuit (1, 2) means comprises: first and second input amplifier means (5, 6), wherein each of the first and second input amplifier means (1, 2) includes first, second and third electrode means, wherein the first electrode means (bases) of the first and second input amplifier means (1,2) are in communication with the input means (5, 6), and wherein the second electrode means (emitters) of the first and second input amplifier means (1, 2) are in communication with each other and a first current source means (13).

Regarding claim 32, wherein the start-up circuit means (3, 4) comprises: first and second start-up amplifier means (3, 4), wherein each of the first and second start-up

amplifier means includes first, second and third electrode means (base, emitter, collector), wherein the first electrode means (bases) of the first and second start-up amplifier means are in communication with a bias input means (base input signals of 3 and 4), wherein the second electrode means of the first and second start-up amplifier means (emitters of 3 and 4) are in communication with each other and with a first current source means (14), and wherein the third electrode means (collector) of the first and second start-up amplifier means (3, 4) are in communication with third electrode means (collector) of first and second input amplifier means (1, 2), respectively.

Regarding claim 34, wherein the amplifier means (Fig. 1) further comprises: feedback means (29, 28) in communication with the output means (32) and second [17, 18] and third [22, 24] current source means, wherein the second and third current source means are in communication with the input (1, 2) and start-up circuit (3, 4) means.

6. Claims 16, 22, 24, 29, 34, and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Muza U.S. patent No. 6,556,081

Regarding claim 16, Fig. 3A and 3B of Muza discloses an electrical circuit, comprising: an amplifier, comprising: an input circuit (INP, INM) in communication with an input of the amplifier (M31, M32); a start-up circuit (M37, M38) in communication with the input circuit, wherein the start-up circuit is configured to generate a start-up signal (D3, E3) to enable subsequent operation of the amplifier; and an output circuit (M35, M36) in communication with an output of the amplifier (A3, B3) and in communication with the input circuit (M31, M32) and the start-up circuit (M37, M38).

Regarding claim 22, Fig. 3B further discloses wherein the amplifier further comprises: a common-mode (A3, B3) feedback circuit (306) in communication with the output (A3, B3) and second and third current sources (Fig. 3A [M33, M34]) wherein the second and third current sources (Fig. 3A [M33, M34]) are in communication with the input (M31, M32) and start-up (M37, M38) circuits.

Regarding claim 24, wherein the amplifier further comprises: fourth and fifth current sources (IB1, IB3) in communication with the input (M31, M32) and start-up circuits (M37, M38) and sixth (IB4) and seventh current sources ([M41-M42] is a current mirror circuit]) in communication with the output (A3, B3) and the output circuit (M35, M36).

Regarding claim 29, Fig. 3A and 3B as applied to claim 16 above, disclosed every aspect of claimed invention.

Regarding claim 34, Muza as applied to claim 22 above, disclosed every aspect of s claimed invention.

Regarding claim 36, Muza as applied to claim 24 above, disclosed every aspect of claimed invention.

7. Claims 39 - 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Minegishi U.S. patent No. 6,462,618.

8. Regarding claim 39, Fig. 6 of Minegishi discloses a method of starting up an electrical circuit, comprising the steps of: applying a first signal (151) to a start-up circuit

Art Unit: 2819

(101, 102) of an amplifier (150) generating a start-up signal (outputs at collectors of 101, 102), using the start-up circuit (101, 102), in response to the first Signal (151) to enable subsequent operation of the amplifier (150); and generating an output signal (162) at an output of the amplifier (150) in response to the start-up signal (151).

Regarding claim 40, wherein the amplifier (150) comprises a differential amplifier ([101, 102], [201, 202]), wherein an input ([101, 102]; [201, 202]) of the amplifier (150) comprises a differential input, and wherein the output (162) of the amplifier (150) comprises a differential output (152).

Regarding claim 41, Fig. 6 of Minegishi further comprising the steps of: comparing (30) a feedback signal (invert input of 30) from the output (162) with a predetermined reference signal (Ground at non-inverted input of 30) to generate a comparison signal (output of 30); and controlling an output level of the output signal of the amplifier using the comparison signal (Col. 4 lines 23 – 36).

Regarding claim 42, Fig. 6 further comprising the steps of: applying the output signal (162) to an input (210) of the amplifier (150) and operating the amplifier in a steady-state mode (Col. 4 lines 23 – 36).

### ***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the



Art Unit: 2819

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 25 and 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wiese et al. as applied to claims 16 and 29 above, and further in view of Uchiyama et al. U.S. Patent No. 6,791,424.

Minegishi as applied to claim 42 above, does not disclose ceasing generation of the start-up signal by the start-up circuit when the operation of the amplifier reaches the steady-state mode.

Fig. 5 of Uchiyama et al. discloses an amplifier circuit (2) having a start up circuit (3) comprising: ceasing generation of the start-up signal by the start-up circuit when the operation of the amplifier reaches the steady-state mode (Col. 9 lines 40 – 46).

Minegishi and Uchiyama et al. are common subject matter start-up circuit for amplifier system. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated taught by Uchiyama into Minegishi for the purpose of providing cease or stop function of the startup circuit when the output of the system reached steady state.

11. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wiese et al. as applied to claim 17 above, Moloudi et al. U.S. patent No. 6, 417,737.

Wiese et al. as applied to claim 17 above, does not discloses wherein the amplifier comprises a Gm cell.

Art Unit: 2819

Fig. 4 of Moloudi et al. discloses a differential amplifier comprises a Gm cell (Col. 11 lines 43 – 44).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have amplifier comprising Gm cell, since Gm cell in the amplifier transistor is a well know and conventional in the art as indicated by Moloudi et al.

12. Claim 28 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wiese et al. as applied to claims 16 and 29 above, Moloudi et al. U.S. patent No. 6, 417,737.

Wiese et al. as applied to claims 16 and 29 above, does not disclose does not disclose wherein the method is compliant with a standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11g and 802.11i.

Fig. 6 of Moloudi et al. discloses an amplifier system is compliant with a standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11g and 802.11i (Col. 6 lines 35 – 37).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a system of Mineghishi to compliant with IEEE 801.11 standard as taught by Moloudi, since every electrical system for using or selling must be compliant with standard regulation.

Art Unit: 2819

13. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Minegishi as applied to claim 42 above, and further in view of Uchiyama et al. U.S. Patent No. 6,791,424.

Minegishi as applied to claim 42 above, does not disclose ceasing generation of the start-up signal by the start-up circuit when the operation of the amplifier reaches the steady-state mode.

Fig. 5 of Uchiyama et al. discloses an amplifier circuit (2) having a start up circuit (3) comprising: ceasing generation of the start-up signal by the start-up circuit when the operation of the amplifier reaches the steady-state mode (Col. 9 lines 40 – 46).

Minegishi and Uchiyama et al. are common subject matter start-up circuit for amplifier system. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated taught by Uchiyama into Minegishi for the purpose of providing cease or stop function of the startup circuit when the output of the system reached steady state.

14. Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Minegishi as applied to claim 39 above, and further in view of Moloudi et al. U.S. Patent No. 6,417, 737.

Minegishi as applied to claim 39 above, does not disclose wherein the method is compliant with a standard selected from the group consisting of 802.1 1, 802.11a, 802.1 1b, 802.11g and 802.11i.

Fig. 6 of Moloudi et al. discloses an amplifier system is compliant with a standard selected from the group consisting of 802.1 1, 802.11a, 802.1 1b, 802.11g and 802.11i (Col. 6 lines 35 – 37).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a system of Mineghishi to compliant with IEEE 801.11 standard as taught by Moloudi, since every electrical system for using or sell must be compliant with standard regulation.

#### ***Allowable Subject Matter***

15. Claims 20, 21, 23, 33 and 35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 20, in addition to other elements in the claim, the prior art does not teach or suggest wherein the output circuit comprises: wherein emitter electrodes of the first and second output transistors are in communication with each other and with a first current source, wherein collector electrodes of the first and second output transistors are in communication with the first and second impedance circuits, respectively, and the output.

With respect to claim 23, in addition to other elements in the claim, the prior art does not teach or suggest wherein the common-mode feedback circuit comprises: first and second resistors in communication with the output and an input of the comparator.

Art Unit: 2819

With respect to claim 33, in addition to other elements in the claim, the prior art does not teach or suggest wherein the output circuit means first and second output amplifier means, comprises: third electrode means of first and second input amplifier means, respectively, wherein the second electrode means of the first and second output amplifier means are in communication with each other and with a first current source means, and wherein the third electrode means of the first and second output amplifier means are in communication with the first and second impedance means, respectively, and the output means.

With respect to claim 35, in addition to other elements in the claim, the prior art does not teach or suggest wherein the feedback means comprises: and first and second resistive means in communication with the output means and an input of the comparator means.

16. Claims 1 – 15 are allowed.

### ***Prior Art***

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

### ***Contact Information***

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

Art Unit: 2819

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Robert Pascal can be reached at (571) 272-1769. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

10/20/05  
Linh Van Nguyen  
Art Unit 2819

